

# LH21256

## NMOS 256K (256K × 1) Dynamic RAM

### FEATURES

- 262,144 × 1 bit organization
- Access times: 100/120/150 ns (MAX.)
- Cycle times: 200/230/260 ns (MIN.)
- Page mode operation
- Power supply: +5 V ± 10%
- Power consumption:  
Operating: 467.5/440/385 mW (MAX.)  
Standby: 27.5 mW (MAX.)
- TTL compatible I/O
- Built-in gated  $\overline{\text{CAS}}$  function
- Separate I/O allows Early-Write action
- Available for read modify write,  $\overline{\text{RAS}}$  only refresh, hidden refresh,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh
- 256 refresh cycle (refreshing time 4 ms)
- Built-in high output bias generator circuit
- Packages:  
16-pin, 300-mil DIP  
16-pin, 325-mil ZIP

### DESCRIPTION

The LH21256 is a 262,144 word × 1 bit dynamic RAM fabricated using N-channel 2-layer polysilicon gate process technology. With multiplexed address inputs and standard 16-pin DIP/ZIP packages, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH21256 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

### PIN CONNECTIONS

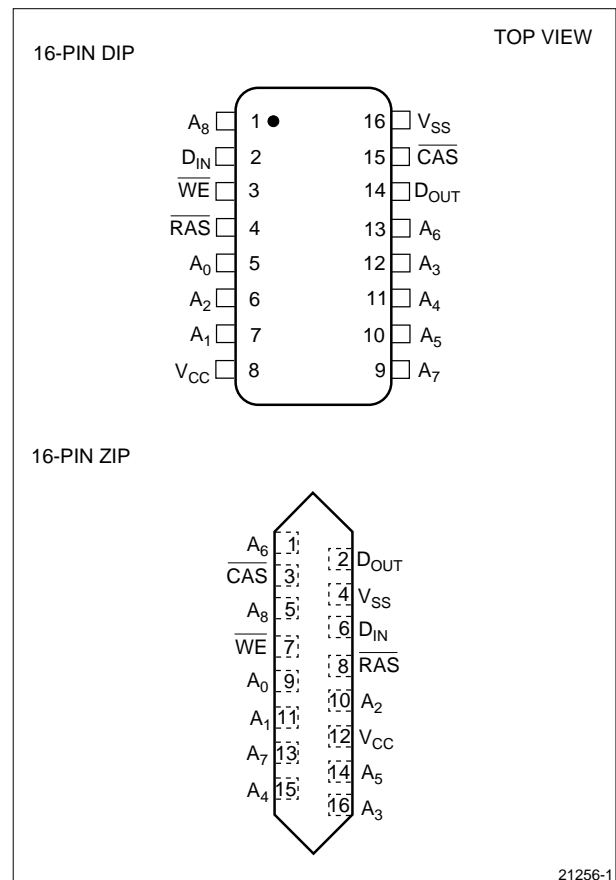


Figure 1. Pin Connections for DIP and ZIP Packages

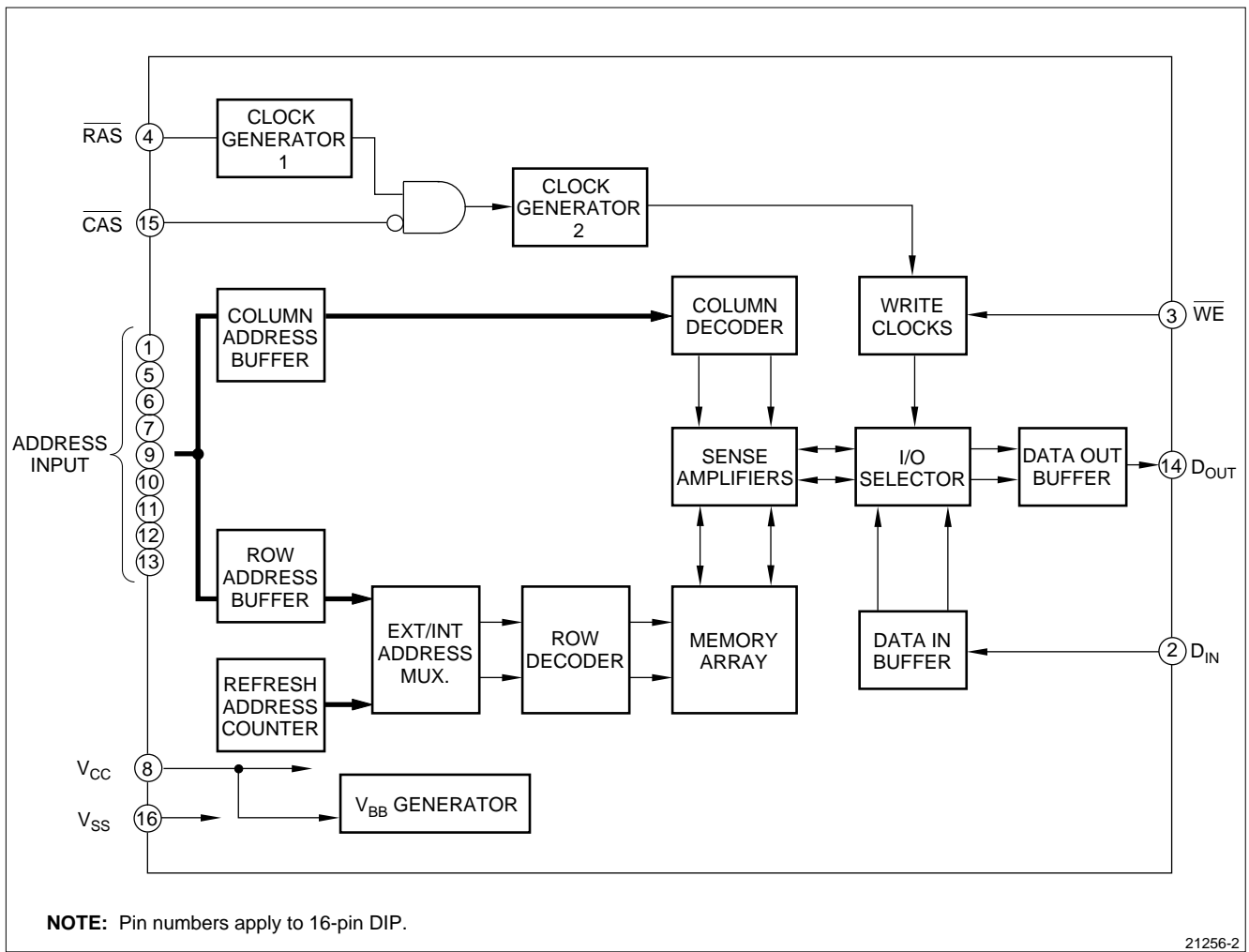


Figure 2. LH21256 Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME
A <sub>0</sub> - A <sub>8</sub>	Address input
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable

SIGNAL	PIN NAME
D <sub>IN</sub>	Data input
D <sub>OUT</sub>	Data output
V <sub>CC</sub>	Power supply (+5 V)
V <sub>SS</sub>	Power supply (0 V)

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V <sub>T</sub>	-1.0 to 7.0	V	1
Output short-circuit current	I <sub>O</sub>	50	mA	
Power consumption	P <sub>D</sub>	1.0	W	
Operating temperature	T <sub>opr</sub>	0 to +70	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	

**NOTE:**

1. Referenced to V<sub>SS</sub>

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = 0 to +70°C)**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	1
	V <sub>SS</sub>	0	0	0		
Input voltage	V <sub>IH</sub>	2.4		6.5	V	1
	V <sub>IL</sub>	-1.0		0.8		

**NOTE:**

1. Referenced to V<sub>SS</sub>

**CAPACITANCE (V<sub>CC</sub> = 5 V ± 10%, T<sub>A</sub> = 0 to +70°C, f = 1MHz)**

PARAMETER	SYMBOL	MIN.	TYPICAL	MAX.	UNIT
Input capacitance	A <sub>0</sub> - A <sub>8</sub> , D <sub>IN</sub> , WE	C <sub>IN1</sub>		7	pF
	RAS, CAS	C <sub>IN2</sub>		10	pF
Output capacitance	D <sub>OUT</sub>	C <sub>OUT</sub>		8	pF

**DC CHARACTERISTICS (V<sub>CC</sub> = 5 V ± 10%, T<sub>A</sub> = 0 to +70°C)**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE	
Average supply current in normal operation	LH21256-10	I <sub>CC1</sub>	—	85	mA	1, 2
	LH21256-12		—	80		
	LH21256-15		—	70		
Average supply current in standby mode	I <sub>CC2</sub>	—	5.0	mA	1	
Average supply current in RAS only refresh time	LH21256-10	I <sub>CC3</sub>	—	65	mA	1, 2
	LH21256-12		—	60		
	LH21256-15		—	55		
Average supply current in page mode	LH21256-10	I <sub>CC4</sub>	—	50	mA	1, 2
	LH21256-12		—	45		
	LH21256-15		—	40		
CAS before RAS average supply current in refresh cycle	LH21256-10	I <sub>CC5</sub>	—	65	mA	1, 2
	LH21256-12		—	60		
	LH21256-15		—	55		
Input leakage current	0 V ≤ V <sub>IN</sub> ≤ 6.5 V 0 V on all other pins	I <sub>I(L)</sub>	-10	10	μA	
Output leakage current	0 V ≤ V <sub>OUT</sub> ≤ 6.5 V Output in high-impedance state	I <sub>O(L)</sub>	-10	10	μA	
Output 'High' voltage	I <sub>OUT</sub> = -5 mA	V <sub>OH</sub>	2.4	—	V	
Output 'Low' voltage	I <sub>OUT</sub> = 4.2 mA	V <sub>OL</sub>	—	0.4	V	

**NOTES:**

1. The output pins are in high-impedance state.
2. I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub>, and I<sub>CC5</sub> depend on the cycle time.

AC CHARACTERISTICS<sup>1, 2, 3</sup> ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0\text{ to }70^\circ\text{C}$ )

PARAMETER	SYMBOL	LH21256-10		LH21256-12		LH21256-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read/write cycle time	$t_{RC}$	200	—	230	—	260	—	ns	
Read write cycle time	$t_{RWC}$	240	—	275	—	310	—	ns	
Access time from $\overline{RAS}$	$t_{RAC}$	—	100	—	120	—	150	ns	4, 6
Access time from $\overline{CAS}$	$t_{CAC}$	—	50	—	60	—	75	ns	5, 6
Output turn-off delay time	$t_{OFF}$	0	30	0	35	0	40	ns	
Rise and fall time	$t_T$	3	35	3	35	3	35	ns	3
RAS precharge time	$t_{RP}$	90	—	100	—	100	—	ns	
RAS pulse width	$t_{RAS}$	100	10,000	120	10,000	150	10,000	ns	
RAS hold time	$t_{RSH}$	50	—	60	—	75	—	ns	
CAS precharge time	$t_{CPN}$	25	—	30	—	35	—	ns	
CAS pulse width	$t_{CAS}$	50	10,000	60	10,000	75	10,000	ns	
CAS hold time	$t_{CSH}$	100	—	120	—	150	—	ns	
CAS hold time (CAS before $\overline{RAS}$ )	$t_{FCH}$	100	—	120	—	150	—	ns	
CAS set up time ( $\overline{CAS}$ before $\overline{RAS}$ )	$t_{FCS}$	20	—	25	—	30	—	ns	
RAS/CAS delay time	$t_{RCD}$	20	50	25	60	30	75	ns	7, 8
CAS/RAS precharge time	$t_{CRP}$	20	—	25	—	30	—	ns	
Row address setup time	$t_{ASR}$	0	—	0	—	0	—	ns	
Row address hold time	$t_{RAH}$	10	—	15	—	20	—	ns	
Column address setup time	$t_{ASC}$	0	—	0	—	0	—	ns	
Column address hold time	$t_{CAH}$	25	—	25	—	45	—	ns	
Column address hold time from $\overline{RAS}$	$t_{AR}$	75	—	95	—	120	—	ns	
Read command setup time	$t_{RCS}$	0	—	0	—	0	—	ns	
Read command hold time	$t_{RCH}$	0	—	0	—	0	—	ns	11
Read command hold time from $\overline{RAS}$	$t_{RRH}$	20	—	20	—	20	—	ns	11
Write command setup time	$t_{WCS}$	0	—	0	—	0	—	ns	10
Write command hold time	$t_{WCH}$	35	—	40	—	45	—	ns	
Write command hold time from $\overline{RAS}$	$t_{WCR}$	85	—	100	—	120	—	ns	
Write command pulse width	$t_{WP}$	35	—	40	—	45	—	ns	
Write command $\overline{RAS}$ lead time	$t_{RWL}$	35	—	40	—	45	—	ns	
Write command $\overline{CAS}$ lead time	$t_{CWL}$	35	—	40	—	45	—	ns	
$\overline{RAS}$ write command delay time	$t_{RWD}$	95	—	120	—	150	—	ns	
$\overline{CAS}$ write command delay time	$t_{CWD}$	45	—	60	—	75	—	ns	
Data input setup time	$t_{DS}$	0	—	0	—	0	—	ns	9
Data input hold time	$t_{DH}$	30	—	30	—	35	—	ns	9
Data input hold time from $\overline{RAS}$	$t_{DHR}$	80	—	90	—	110	—	ns	
Refresh time	$t_{REF}$	—	4	—	4	—	4	ms	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	$t_{RPC}$	0	—	0	—	0	—	ns	

## NOTES:

- For proper operation, at least 500  $\mu\text{s}$  of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
- AC characteristics assume  $t_T = 5\text{ ns}$ .
- Timing measurements are referenced to  $V_{IH}$  (MIN.) and  $V_{IL}$  (MAX.). ( $t_T$  refers to the transition time between  $V_{IH}$  and  $V_{IL}$ .)
- Only when  $t_{RCD} \leq t_{RCD}(\text{MAX.})$ . If  $t_{RCD} > t_{RCD}(\text{MAX.})$ ,  $t_{RAC}$  will increase by  $(t_{RCD} - t_{RCD}(\text{MAX.}))$
- When  $t_{RCD} \geq t_{RCD}(\text{MAX.})$ .
- Load condition for 2TTL + 100 pF.
- $t_{RCD}(\text{MAX.})$  is the maximum point for  $t_{RCD}$  where  $t_{RAC}(\text{MAX.})$  is ensured, and does not represent a limit of operation. If  $t_{RCD}(\text{MAX.}) \leq t_{RCD}$ , the access time is controlled by  $t_{CAC}$ .
- $t_{RCD}(\text{MIN.}) = t_{RAH}(\text{MIN.}) + 2t_T + t_{ASC}(\text{MIN.})$ .
- $t_{DS}$  and  $t_{DH}$  are given with respect to the fall of  $\overline{CAS}$  in the Early-Write cycle and the fall of  $\overline{WE}$  in the read/write cycle and the Read-Modify-Write cycle.
- $t_{WCS}$ ,  $t_{CWD}$  and  $t_{RWD}$  are the specified points of the operating mode, and do not represent a limit of operation. When  $t_{WCS} \geq t_{WCS}(\text{MIN.})$ , it comes into early write cycle with  $D_{OUT}$  pin coming into high-impedance state. When  $t_{CWD} \geq t_{CWD}(\text{MIN.})$  and  $t_{RWD} \geq t_{RWD}(\text{MIN.})$ , it comes into the read/write cycle with the output data becoming the information for the selection cell. Timing other than the above-mentions will give undefined value of output.
- The operation is ensured when either  $t_{RCH}$  or  $t_{RRH}$  is satisfied.

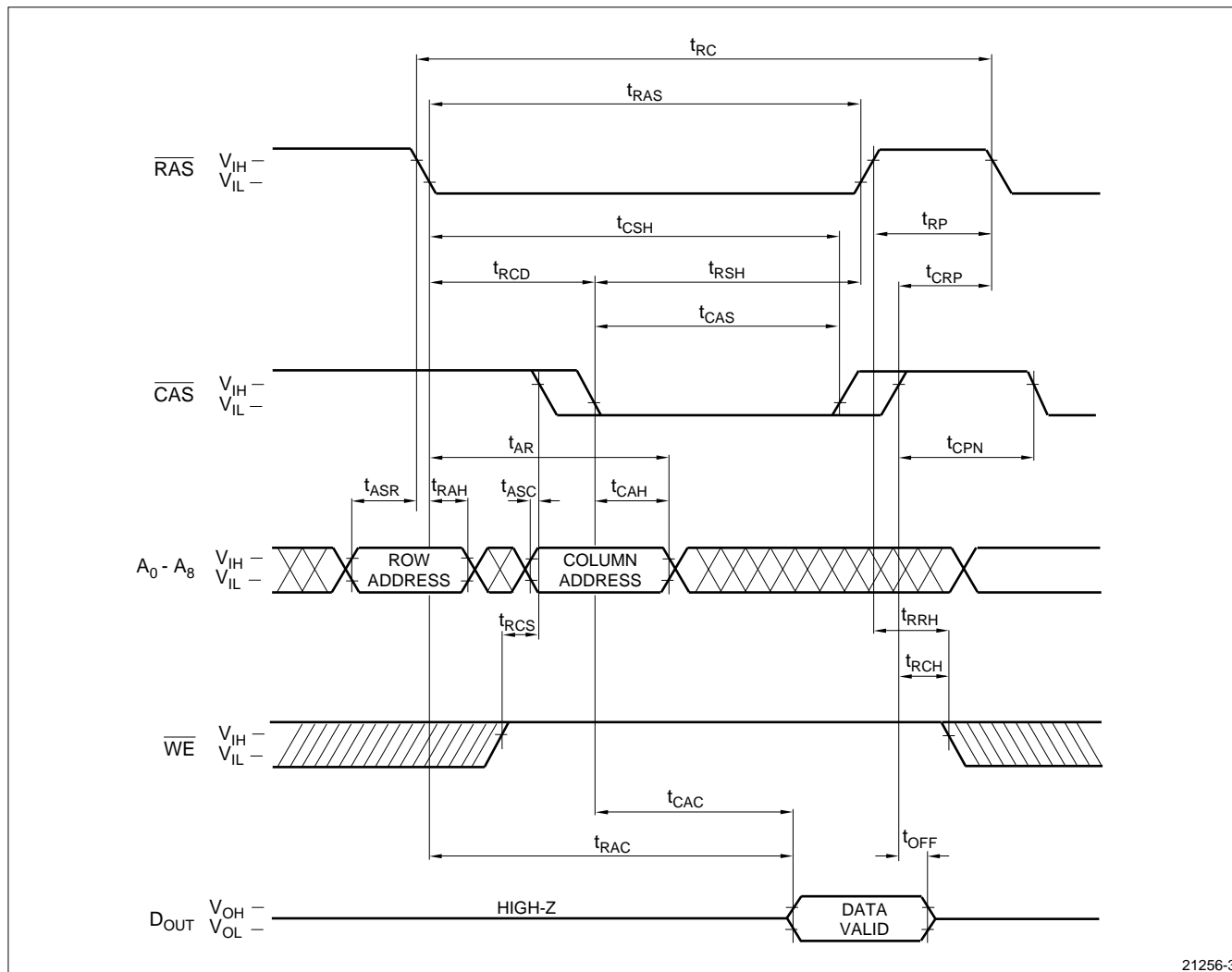
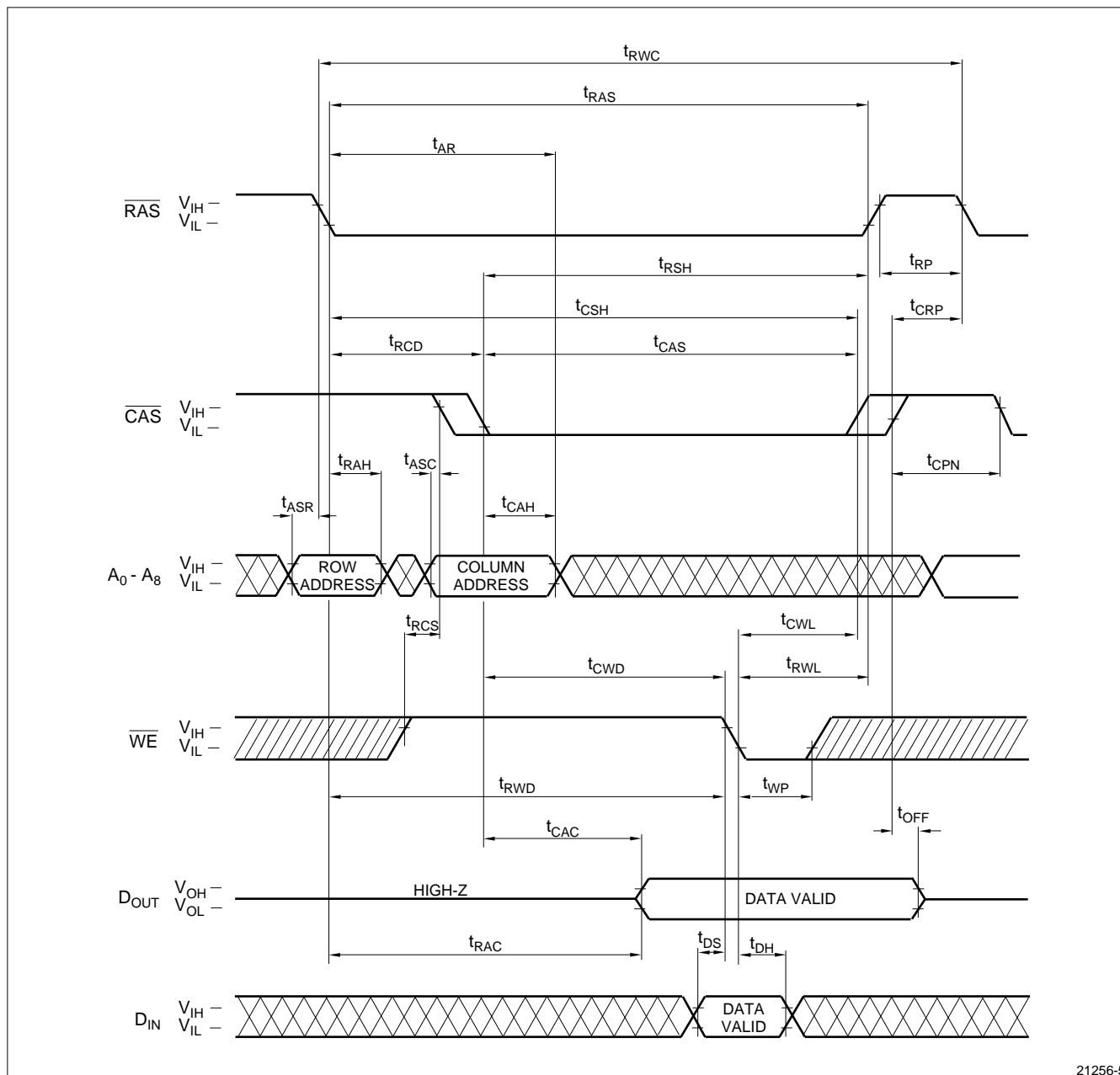


Figure 3. Read Cycle





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Figure 5. Read-Write/Read-Modify-Write Cycle

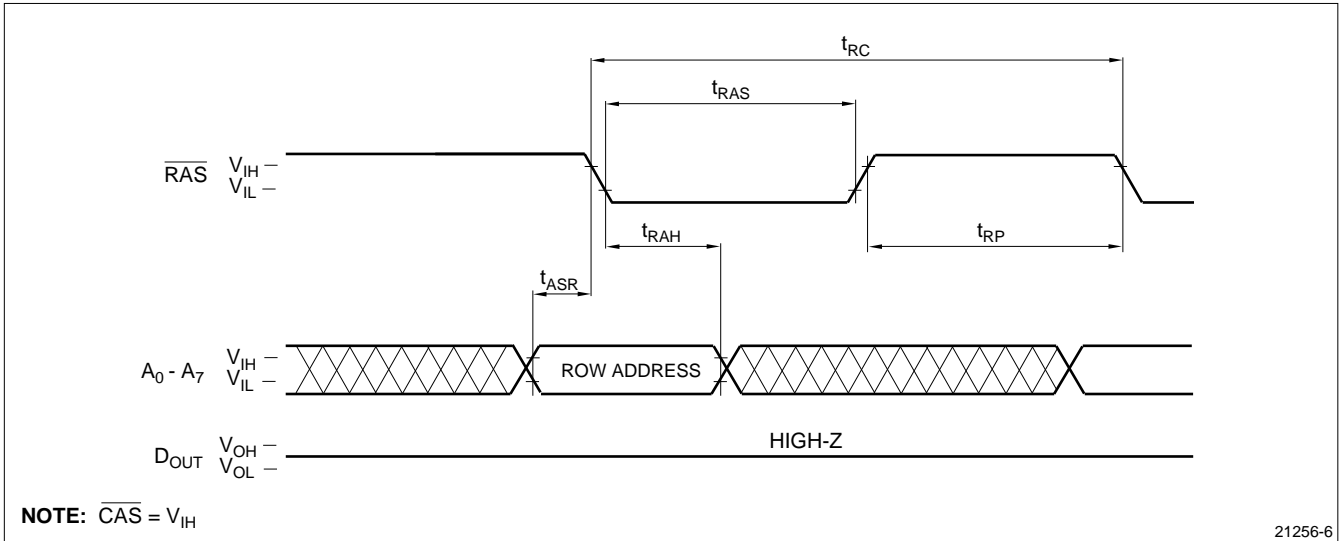


Figure 6.  $\overline{\text{RAS}}$  Only Refresh Cycle

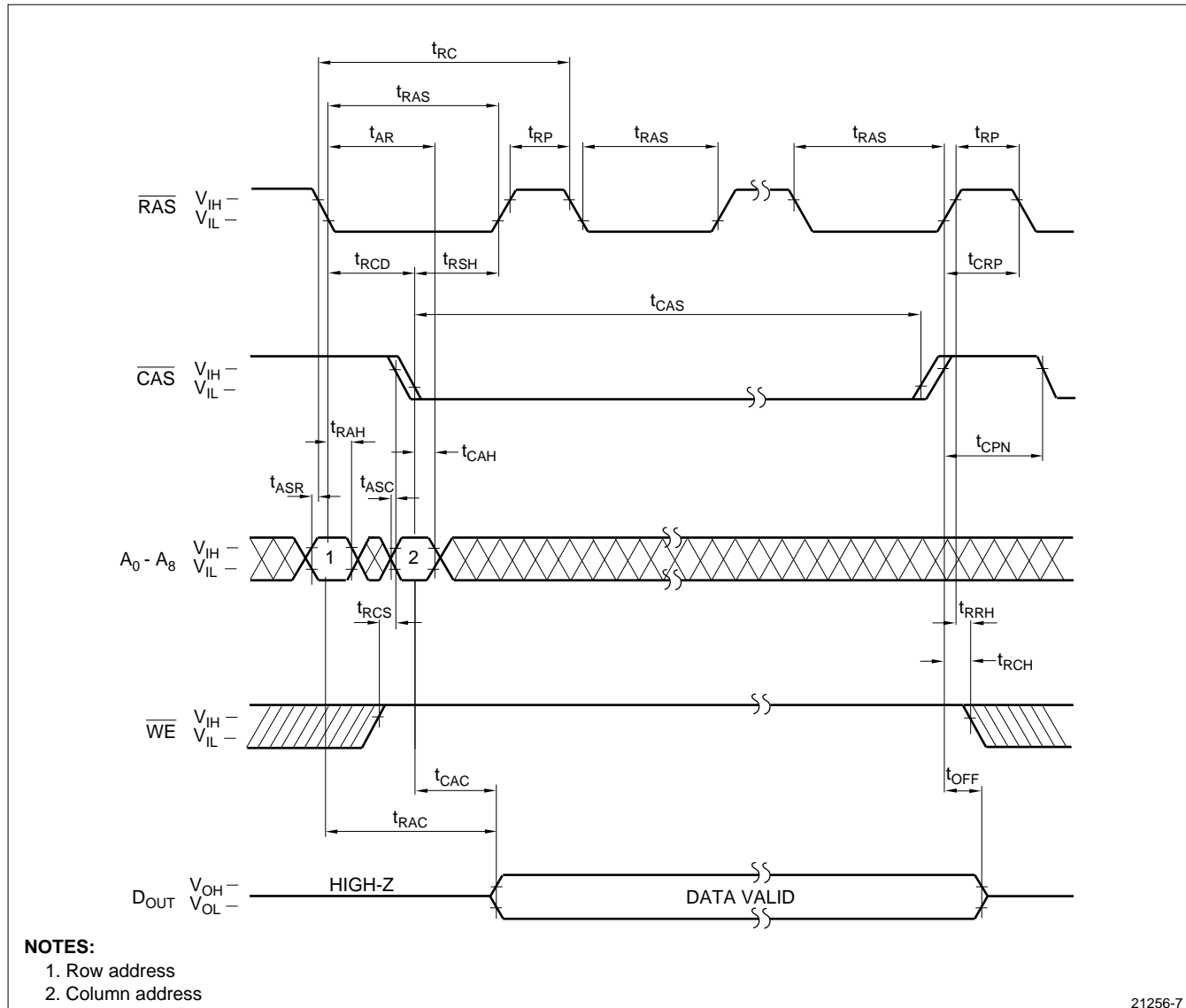


Figure 7. Hidden Refresh Cycle



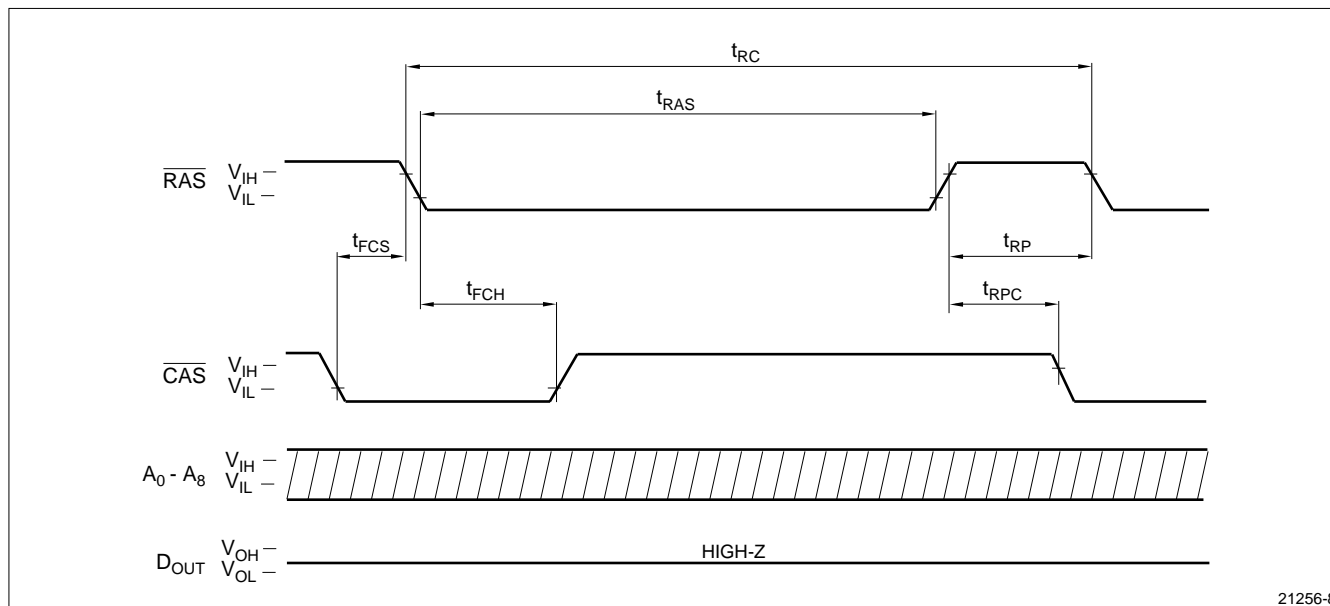
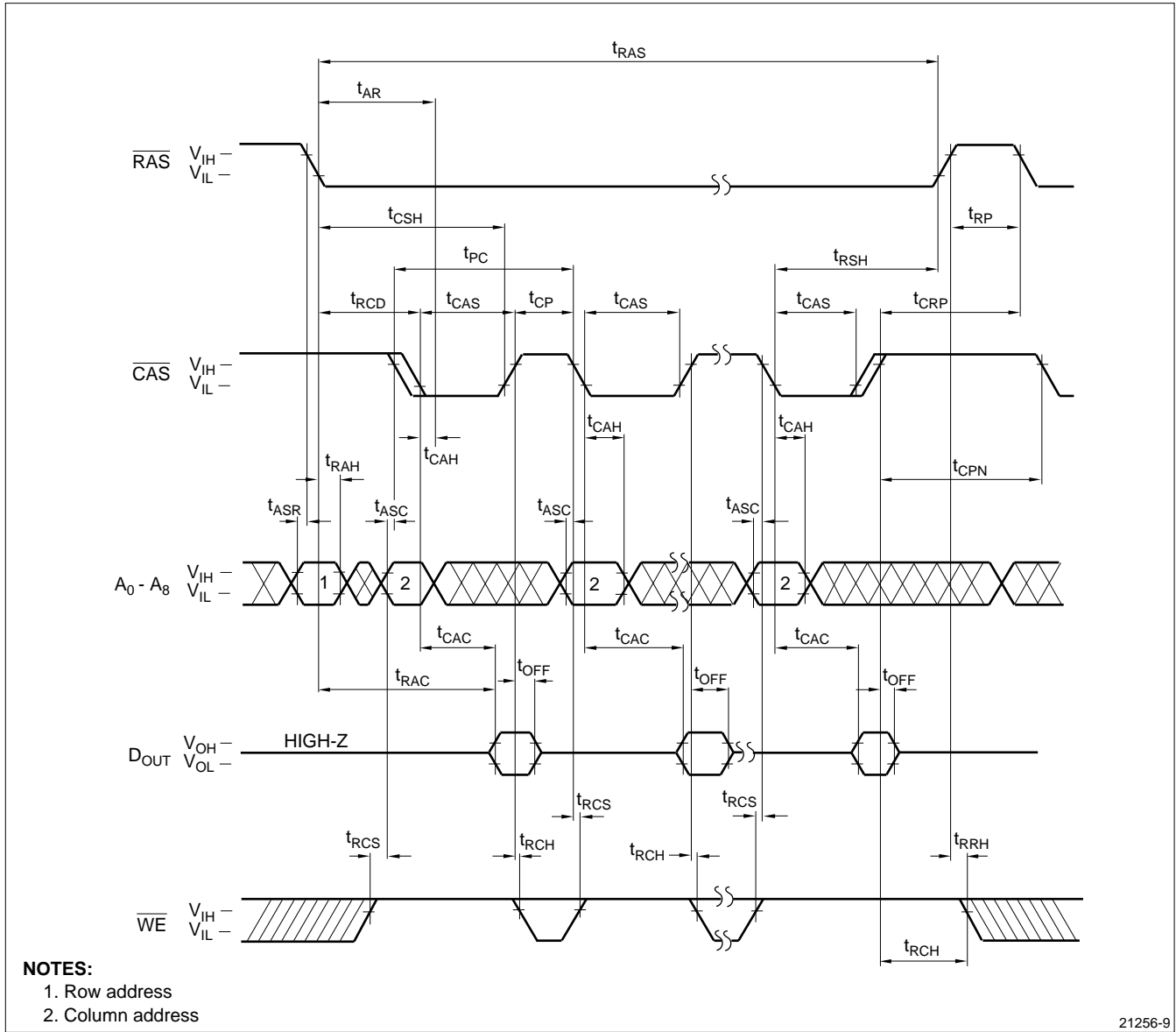


Figure 8.  $\overline{\text{CAS}}$  Before  $\overline{\text{RAS}}$  Refresh Cycle

**PAGE MODE CHARACTERISTICS ( $V_{CC} = 5 V \pm 10\%$ ,  $T_A = 0$  to  $+70^\circ C$ )**

PARAMETER	SYMBOL	LH21256-10		LH21256-12		LH21256-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Page mode cycle time	$t_{PC}$	100	—	120	—	145	—	ns	
CAS precharge time	$t_{CP}$	40	—	50	—	60	—	ns	



**Figure 9. Page Mode Read Cycle**

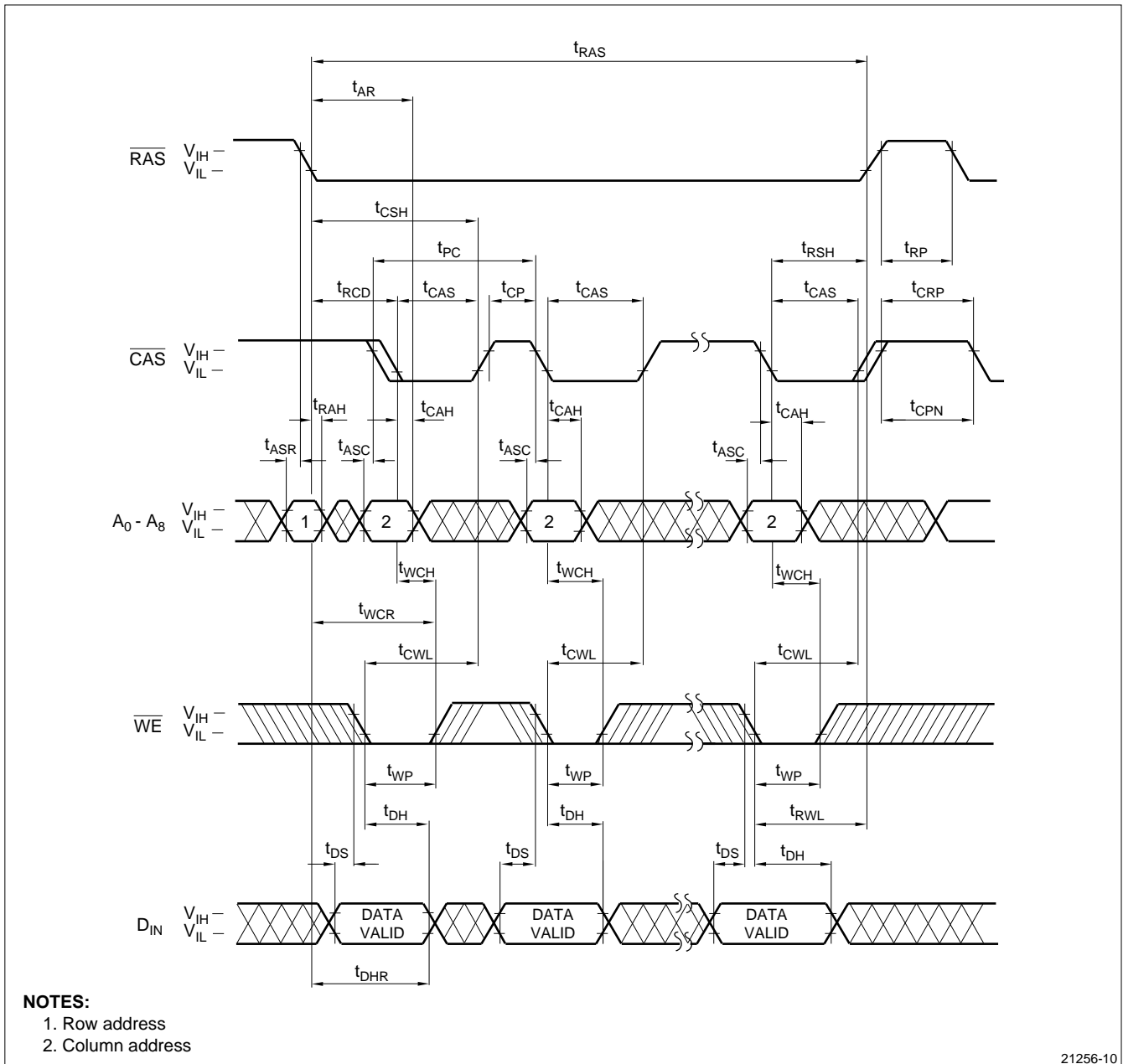
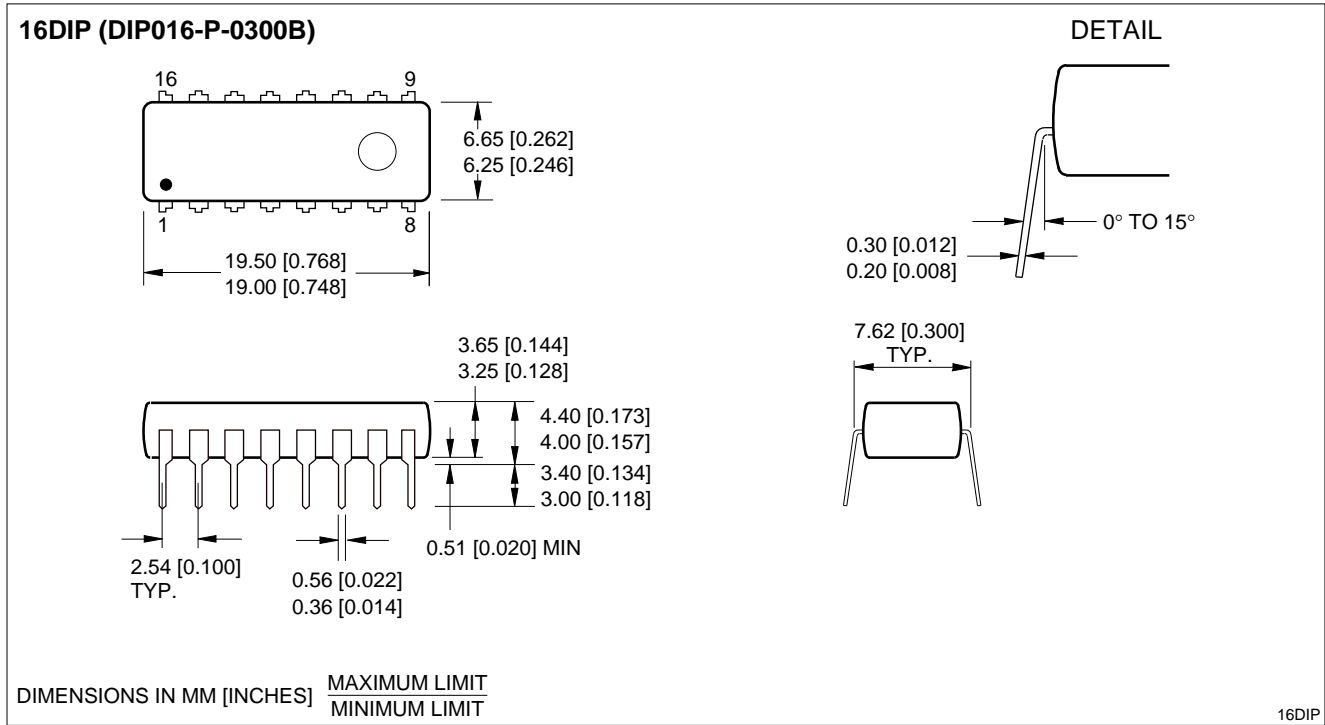
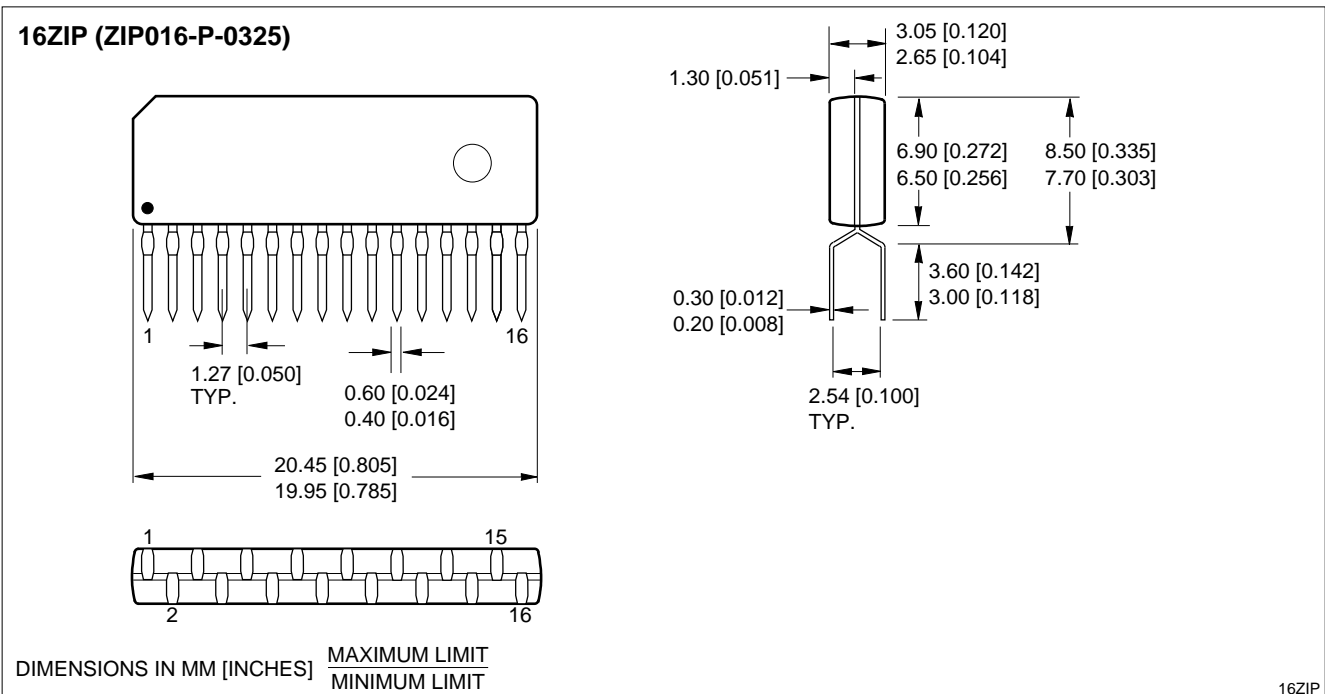


Figure 10. Page Mode Write Cycle

PACKAGE DIAGRAMS

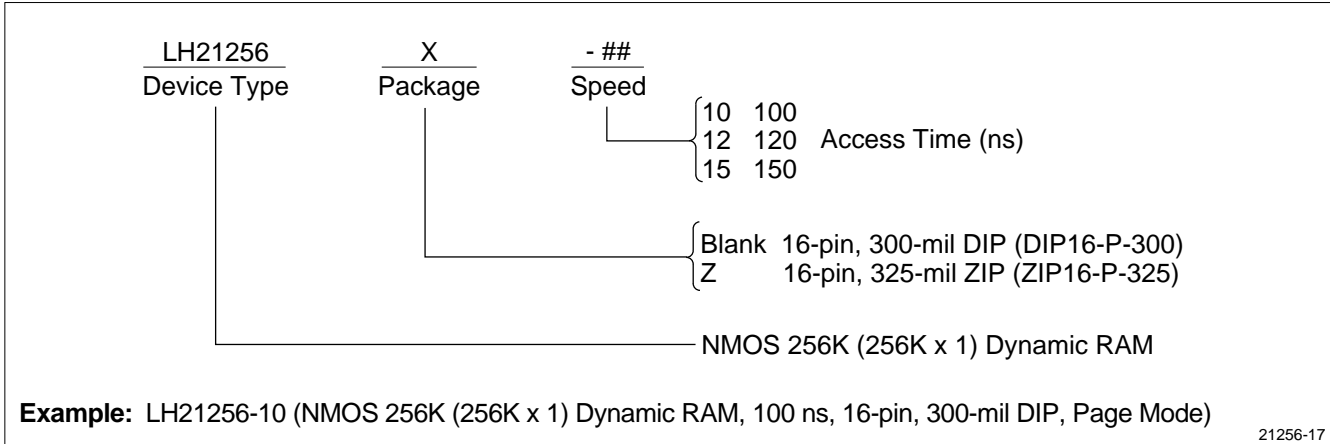


16-pin, 300-mil DIP



16-pin, 325-mil ZIP

**ORDERING INFORMATION**



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